IN THE CLAIMS

Please amend the claims as follows:

1. (Cancelled)

2. (Currently Amended) A module comprising:

a semiconductor device;

a phase adjustment circuit which receives a phase adjustment signal output from said semiconductor device and a first clock supplied from an exterior of said module, and generates a second clock; and

an output circuit that is provided in the semiconductor device and generates the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a phase of the second clock such as to fix relative phase difference between the phase adjustment signal and the first clock, wherein

said semiconductor device is a semiconductor memory device including an output buffer from which data stored in memory cells are output in synchronism with the second clock, and wherein

a delay of the data along a path from the semiconductor device to the exterior of the module is substantially the same as a delay of the phase adjustment signal along a path from the semiconductor device to the phase adjustment circuit.

3. (Cancelled)

4. (Currently Amended) A module comprising:

semiconductor devices;

a phase adjustment circuit generating a second clock based on ~~so that~~ a phase adjustment signal output from a first semiconductor device that is one of the semiconductor devices and a first clock supplied from an exterior of the module ~~have a predetermined phase relationship~~, the second clock being supplied to the semiconductor devices; and

a wiring board on which the semiconductor devices and the phase adjustment circuit are mounted,

the first semiconductor device including an output circuit generating the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a phase of the second clock such as to fix a relative phase difference between the phase adjustment signal and the first clock, wherein

each of said semiconductor devices is a semiconductor memory device including an output buffer from which data in memory cells are output in synchronism with the second clock, and wherein

a delay of the data along paths from the semiconductor devices to the exterior of the module is substantially the same as a delay of the phase adjustment signal along a path from the first semiconductor device to a phase adjustment circuit.

5. (Previously Presented) The module as claimed in claim 4, wherein the module comprises first data lines over which data output from the semiconductor devices are transferred, and a second data line over which the phase adjustment signal output from the first semiconductor device is transferred,

the first and second data lines being provided on the wiring board.

6. (Original) The module as claimed in claim 4, wherein the module comprises

first data lines over which data output from the semiconductor devices are transferred, and a second data line over which the phase adjustment signal output from the first semiconductor device is transferred,

the first and second data lines being provided on the wiring board.

7. (Original) The module as claimed in claim 6, wherein the first and second data lines are arranged on an identical side of the wiring board.

8. (Original) The module as claimed in claim 6, wherein the first and second data lines are arranged on an identical side of the wiring board.

9. (Original) The module as claimed in claim 5, wherein the first and second data lines are arranged on opposite sides of the wiring board so that the semiconductor devices are sandwiched between the first and second data lines.

10. (Original) The module as claimed in claim 6, wherein the first and second data lines are arranged on opposite sides of the wiring board so that the semiconductor devices are sandwiched between the first and second data lines.

11. (Original) The module as claimed in claim 5, wherein the first and second data lines have a substantially identical delay amount.

12. (Original) The module as claimed in claim 6, wherein the first and second data lines have a substantially identical delay amount.

13. (Original) The module as claimed in claim 5, wherein the first and second data lines have a length that allows their delay amounts to be negligible.

14. (Original) The module as claimed in claim 6, wherein the first and second data lines have a length that allows their delay amounts to be negligible.

15. (Previously Presented) The module as claimed in claim 4, further comprising a terminal that is provided on the wiring board and is used to output the phase adjustment signal to an outside of the module.

16. (Previously Presented) The module as claimed in claim 4, wherein the first semiconductor device generates the phase adjustment signal in accordance with a predetermined signal given from an outside of the first semiconductor device.

17. (Previously Presented) The module as claimed in claim 4, wherein:

the semiconductor devices including the first semiconductor device have an identical circuit configuration; and

the first semiconductor device has an output circuit that receives an external instruction that instructs the first semiconductor device to generate the phase adjustment signal.

18. (Previously Presented) The module as claimed in claim 4, wherein the first clock is supplied from an outside of the module.

19. (Previously Presented) The module as claimed in claim 4, further comprising a circuit generating the first clock from an external clock.

20. (Previously Presented) The module as claimed in claim, wherein each of the semiconductor devices comprises a programmable delay circuit that delays the second

clock.

21. (Previously Presented) The module as claimed in claim 4, wherein the semiconductor devices comprise semiconductor memory devices.

22. (Previously Presented) The module as claimed in claim 4, wherein the phase adjustment circuit generates the second clock from dummy output data output by the first semiconductor device.

23. (Previously Presented) The module as claimed in claim 4, further comprising a second phase adjustment circuit generating a third clock so that the third clock and the first clock have a predetermined phase relationship, the third clock being supplied to the semiconductor devices.

24. (Original) The module as claimed in claim 23, wherein the first clock corresponds to the third clock.

25. (Currently Amended) A system comprising:

modules;

a wiring board on which the modules are mounted; and

a dummy output load line serving as loads of dummy output data output from the modules, wherein the modules comprise a module including;

a semiconductor devices, one of which is a first semiconductor device that outputs a phase adjustment signal; and

a phase adjustment circuit which receives the phase adjustment signal output from said first semiconductor device and a first clock supplied from an exterior of said module,

and generates a second clock, the second clock being supplied to the semiconductor devices~~; and~~

~~a wiring board on which the semiconductor devices and the phase adjustment circuit are mounted~~,

the first semiconductor device including an output circuit generating the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a phase of the second clock such as to fix a relative phase difference between the phase adjustment signal and the first clock, wherein

each of said semiconductor devices is a semiconductor memory device including an output buffer from which data stored in memory cells are output in synchronism with the second clock, and wherein

a delay of the data along paths from the semiconductor devices to the exterior of the module is substantially the same as a delay of the phase adjustment signal along a path from the first semiconductor device to the phase adjustment circuit.

26. (Original) The system as claimed in claim 25, wherein the dummy output load line is provided in common to the modules.

27. (Original) The system as claimed in claim 25, wherein the dummy output load line comprises parts respectively provided to the modules.